BOOTSTRAP CAPACITOR REFRESH CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to power switching circuits and, in particular, to driver circuits for driving power switching circuits. In particular, the present invention relates to a bootstrap capacitor power supply refresh circuit utilized in a driver circuit for driving a power switching circuit, for example, a half bridge power switching circuit driving a load.

Bootstrap capacitors are often employed in driver circuits to provide an additional fkiatubg voltage from an existing power supply or from an existing voltage source or from a pulsed signal source. In particular, as shown in Fig. 1, which shows a driver IC for driving a half bridge switching circuit comprising two power MOSFETs M1 and M2 driving a load, as shown there, the half bridge transistors M1 and M2 are arranged between a voltage source VBAT and ground. The voltage supply is also provided to the driver IC (IC) at a voltage input VCC to provide power to the driver IC. VBAT may be a different, higher voltage than VCC, or it may be the same voltage. Typically, VCC is different than VBAT because of high voltage spikes on VBAT. VCC may be derived from VBAT by an internal or external regulator circuit. The driver IC includes a driver HO and a driver LO which drive the respective high side and low side transistors M1 and M2. In addition, an external bootstrap capacitor CBOOT is provided between a terminal VB and the terminal VS which is coupled to the load and which is the common connection between the transistors M1 and M2. A supply voltage VBOOT is thus provided across the bootstrap capacitor. A diode D is disposed either internally to the IC or external to it to allow the bootstrap capacitor CBOOT to charge up from VCC when

transistor M2 is on. The bootstrap supply is used to suply a votlage to the high side driver.

A problem arises when there is a permanent conduction of transistor M1. By "permanent conduction" is meant a relatively lengthy on time for transistor M1, for example, more than 200 usecs. In such a circumstance, transistor M2 is off and accordingly, the bootstrap capacitor cannot charge through transistor M2 during such operation. Accordingly, the circuit of Fig. 1 cannot be used if transistor M1 has relatively lengthy on times, for example conduction times greater than 200 usec. Transistor M2 will simply not be on long enough to allow the bootstrap capacitor to charge up and therefore provide a power source to circuits either internal to the IC or external to it that are powered by VBOOT.

It is therefore necessary to provide a solution to this problem, and particularly one that is useful in automotive applications.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a solution to the problem of the prior art bootstrap capacitor circuit wherein there is insufficient time during certain modes of operation of the switching transistors for the bootstrap capacitor to maintain a required charge.

The above and other objects of the present invention are achieved by a bootstrap capacitor charging circuit comprising first and second power switching transistors arranged in a half bridge arrangement such that the first and second transistors are disposed between a high side potential and a low side potential, a driver circuit for driving the first and second transistors, a bootstrap capacitor adapted to be charged from a potential source and for providing a voltage source to power an electronic circuit, a charging circuit providing a charging path from one of said high and low side potentials to said bootstrap capacitor, first and second series

connected switches arranged between a common node of said first and second transistors and one of said high and low side potential, the bootstrap capacitor having a first terminal coupled to be charged by said charging circuit and a second terminal coupled to a common node between said first and second series connected switches; and a control circuit operating in first and second modes, wherein in a first mode when said first and second power switching transistors are switching at a rate above a predetermined frequency, a first of said switches connected to said common node of said first and second power switching transistors is controlled on and said second switch is controlled off; and wherein, when said first power switching transistor is on for a duration of time exceeding a preset duration, said control circuit operates in a second mode wherein said first and second switches are alternately turned on and off for first and second predefined periods of time whereby the bootstrap capacitor charges through said second switch and said charging circuit during the second predefined period of time.

The above and other objects are also achieved by a method for charging a bootstrap capacitor in a circuit comprising first and second power switching transistors arranged in a half bridge arrangement such that the first and second transistors are disposed between a high side potential and a low side potential, a driver circuit for driving the first and second transistors; a bootstrap capacitor adapted to be charged from a potential source and for providing a voltage source to power an electronic circuit; a charging circuit providing a charging path from one of said high and low side potentials to said bootstrap capacitor, first and second series connected switches arranged between a common node of said first and second transistors and one of said high and low side potential; the bootstrap capacitor having a first terminal coupled to be charged by said charging circuit and a second terminal coupled to a common node between said first and second series connected switches; and a control circuit for controlling the first and second switches, the method

comprising operating said first and second switches in a first mode when said first and second power switching transistors are switching at a rate above a predetermined frequency, such that a first of said switches connected to said common node of said first and second power switching transistors is controlled on and said second switch is controlled off; and operating said first and second switches in a second mode when said first power switching transistor is on for a duration of time exceeding a preset duration, such that said first and second switches are alternately turned on and off for first and second predefined periods of time whereby the bootstrap capacitor charges through said second switch and said charging circuit during the second predefined period of time.

Other objects, features and advantages of the invention will become apparent from the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWING(S)

The invention will now be described in greater detail in the following detailed description with reference to the attached drawings in which:

Fig. 1 shows a prior art circuit employing a bootstrap capacitor power supply;

Fig. 2 shows the circuit according to the present invention;

Fig. 3 shows a timing diagram useful for explaining the present invention.

Other objects, features and advantages of the present invention will become apparent from the detailed description that follows.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Fig. 2, a driver integrated circuit (IC) for a half bridge switching transistor arrangement comprising transistors M1 and M2 series connected between power supply VBAT and ground is shown. The load is connected between

the common node between transistors M1 and M2 comprising the point VS and ground.

The driver integrated circuit IC includes the high side and low side drivers HO and LO for each of the high side and low side power transistors M1 and M2. In addition, the driver IC includes a ballast regulator 10 comprising a transistor, for example, a bipolar NPN transistor 12 and a current source 14 as well as a zener diode 16 which may be a 6.6 volt zener diode in the illustrated embodiment. In addition, the bootstrap capacitor CBOOT is externally connected and separated from VS. The bootstrap capacitor is connected between the terminals VB and VB1 of the driver IC. Terminal VB1 is connected to the anode of zener diode 16 which is also connected to a switch SW2 which is connected to the common terminal and thence to ground. In addition, switch SW1 is connected between VS and VB1 as shown. Switches SW1 and SW2 are semiconductor switches, e.g., MOSFETs or bipolar transistors.

In addition, a control circuit 18 is provided which provides output signals SW1 and SW2 (Fig. 3) to control the switching action of the switches SW1 and SW2.

The circuit operates as follows. During normal operation, for conduction times of M1 less than 200 usec., controller 18 operates in a first mode (MODE 1 - Fig. 3) such that switch SW1 is always on and switch SW2 is always off. As such, the circuit operates like a normal bootstrap power supply and the capacitor CBOOT is charged through M2 and the switch SW1 and the ballast regulator 10 to VBAT when M2 is on. The ballast regulator 10 provides a regulated voltage at the emitter of transistor 12 of approximately 6 volts, based on a 6.6 volt zener diode 16.

When the transistor M1 is on for periods of time greater than 200 usec., in the prior art circuit there is insufficient time for the capacitor to charge through M2. In such a case, control circuit 18 operates in a second mode (MODE 2 - Fig. 3). Circuit 18 has included therein an oscillator comprising a 2 kHz oscillator, for example.

Every 500 usec, as shown in Fig. 3, switch SW1 is turned off and switch SW2 is turned on for a time period of approximately 10 μsec. The bootstrap capacitor CBOOT is charged up through SW2 coupled to ground and through the ballast regulator to VBAT. During this time, the gate of M1 may be left floating.

The present invention thus provides a simple and reliable way to charge a bootstrap capacitor so that power can reliably be provided to circuits coupled and powered by the bootstrap capacitor for all modes of operation of the power switching circuit, including when the high side transistor is in a permanent state of conduction.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention should be limited not by the specific disclosure herein, but only by the appended claims.